



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,585	09/11/2003	Shunpei Yamazaki	0756-7196	7079
31780	7590	10/17/2005	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			DOTY, HEATHER ANNE	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/659,585

Applicant(s)

YAMAZAKI ET AL.

Examiner

Heather A. Doty

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-50 is/are pending in the application.
- 4a) Of the above claim(s) 4,5,7,8,10,11,13,14 and 16 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2,3,6,9,12,15 and 17-50 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/11/03, 12/12/03 \*
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: IDS 3/22/04, 7/25/05 \*

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election of 2, 3, 6, 9, 12, 15, and 17 in the reply filed on 7/15/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Additionally, the examiner agrees that claim 1 is generic to all species, so claims 1, 2, 3, 6, 9, 12, 15, 17, and 18-50 are subject to examination.

### ***Information Disclosure Statement***

The examiner is unable to locate in the application file the non-patent literature by Tsutsui et al. listed in the Information Disclosure Statement filed 9/11/2003. Therefore only the abstract has been considered, a copy of which is included with this Office action.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Teong (U.S. 5,693,563) in view of Moritz et al. (U.S. 4,659,650) and Douglas (U.S. 4,100,499).

Regarding claim 1, Teong teaches a method of manufacturing a semiconductor device comprising the steps of:

forming a wiring comprising at least a laminate of a first conductive film with a property as a barrier and a second conductive film containing copper as its main component, said step of forming a wiring including the steps of:

- (i) forming a first conductive film (barrier layer 4 in Fig. 1; column 4, lines 3-6) over an insulating surface (1 in Fig. 1; column 3, lines 61-63);
- (ii) etching the first conductive film (column 4, lines 7-9);
- (iii) forming the second conductive film on the first conductive film (copper layer 8 in Fig. 4; column 4, lines 26-29); and
- (iv) reducing a width of the second conductive film (column 4, lines 29-33).

Teong does not teach that the copper layer is formed through an opening of a mask or that the width of the second conductive film is reduced with dry etching.

Moritz et al. teaches depositing copper through an opening of a lift-off mask (column 5, lines 42-52) using a method that produces low and uniform contact resistance (column 2, lines 31-32).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Teong and further deposit the copper layer through the lift-off mask taught by Moritz et al. The motivation for doing so at the time of the invention would have been to produce low and uniform contact resistance between layers, as taught by Moritz et al.

Douglas teaches a method of dry-etching copper (column 2, lines 50-55) that offers the advantage over wet-etching processes of not contaminating the integrated

Art Unit: 2813

circuit (column 1, lines 56-59), and additionally offers greater control in etching features (column 1, lines 63-66; column 3, lines 6-7).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Teong and Moritz et al. together, and also use dry etching to reduce the width of the second conductive layer, as taught by Douglas. The motivation for doing so at the time of the invention would have been because this etching method does not contaminate the device and offers greater control in etching features than wet etch processes do, as expressly taught by Douglas.

***Allowable Subject Matter***

Claims 2, 3, 6, 9, 12, 15, and 17-50 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest, in combination with the other claimed limitations, a method of manufacturing a semiconductor device that comprises forming a wiring according to the method taught by claim 1 and then using the wiring as a mask to form an impurity region. Nakanishi et al. (U.S. 6,265,247) teaches a method of manufacturing a semiconductor device comprising substantially all of the steps recited in claims 2 and 18, except that the gate used as a mask to form an impurity region is formed through sputtering a metal with a high melting point such as chromium or molybdenum. However, there is no reason to combine this teaching with the combined teachings of Teong, Moritz et al., and Douglas to arrive at the invention as claimed in claims 2, 3, 6, 9, 12, 15, and 17-50. The method taught by Teong and modified by

Moritz et al. and Douglas (see U.S.C. 103(a) rejection above) is primarily a dual-damascene method, which would not be appropriate to use as a mask to form an impurity region.


### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800